1 Wafer fabrication

1.1 Wafer fabrication

1.1.1 Wafer separation and surface refinement

At first the single crystal is turned to a desired diameter and then bedight with one or two flats. The larger, first flat allows an precise alignment of the wafer during manufacturing. The second flat is used to detect the type of the wafer (crystal orientation, p-/n-type doped), but is not always used. Wafers with a diameter of 200 mm or above use a notch instead. This tiny notches on the edge of the disk also provide an alignment of the wafer, but take up much less costly wafer surface.

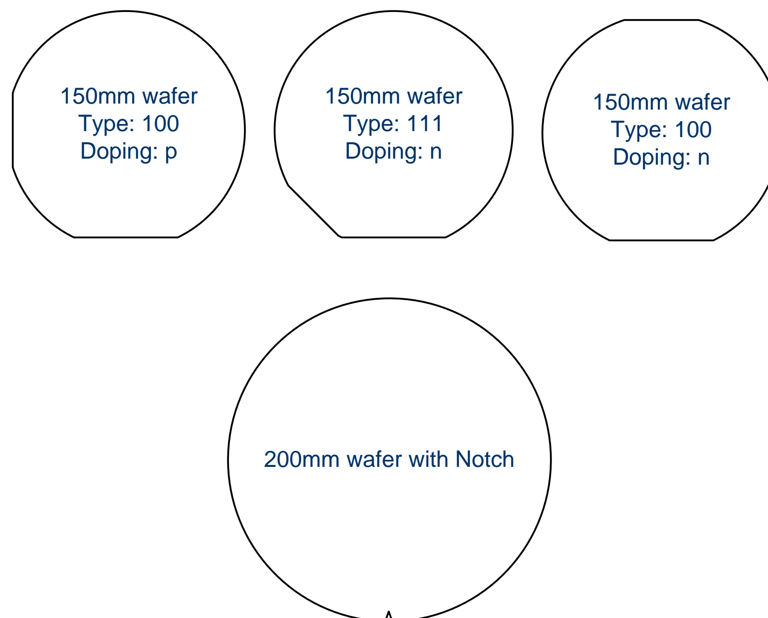

Fig. 1.1: Different types of wafers

Sawing:

With an annular saw, whose cutting edge is filled with diamond splinters, the single

crystal is sawn into thin discs = wafer. The saw provides a high accuracy during sawing without bumps. Up to 20 % of the crystal rod is lost due to the width of the saw blade. However, nowadays more often wire saws are used, in which multiple wafers can be cut at once from the staff. Therefore a long wire, which is wetted with a suspension of silicon carbide grains and a carrier (glycol or oil), is lead through rotating rollers. The silicon crystal is drained into the wire grid and thus cut into single wafers. The wire moves in counterstep with about 10 m/s and has a typically thickness of 0.1-0.2 mm.

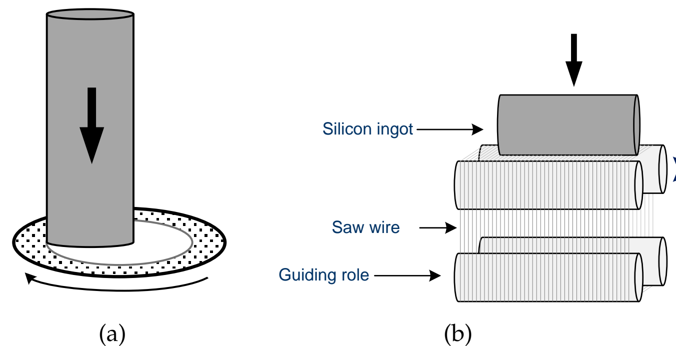

Fig. 1.2: Annular and wire saw

After sawing, the slices have a rough surface, and due to mechanical stress damages in the crystal lattice. For finishing the surface, the wafers pass several process steps.

Lapping:
Using granular abrasives (e.g. aluminum) 50 microns (0.05 mm) of the wafer surface are removed on a rotating steel disc. The grain size is reduced in stages, but the surface is re-injured due to the mechanical treatment. The flatness after lapping is about 2 microns.

Beveling of the edge:
In subsequent processes, the discs must have no sharp edges, as deposited layers may flake off otherwise. Therfore the bevel of the wafers are rounded with a diamond cutter.

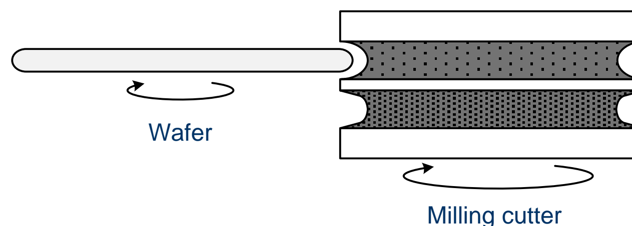

Fig. 1.3: Beveling

Etching:
In an additional wet etch process, with a mixture of hydrofluoric, acetic, and nitric acid, 50 microns are removed. Because this is a chemical process, the surface is not damaged. Crystal defects are permanently resolved.

Polishing:
This is the final step of surface refinement. At the end of the polishing step, the wafers do not have a bump of more than 3 nm (0.000003 mm). The wafers are treated with a mixture of sodium hydroxide NaOH, water, and silicon oxide grains. The oxide removes additional 5 microns from the surface, the hydroxide removes machining marks caused by the oxide grain.

1.1.2 Historical development of the wafer size

The manufacture of integrated circuits on silicon wafers started in the mid 1960s on wafers with a diameter of 25 mm. Nowadays, in modern semiconductor manufacturing wafers with a diameter of 150-300 mm are used. By 2012 the mass production of microchips on wafers with a diameter of 450 mm is expected; prototypes have already been produced for research purposes. The wafer surface is then increased by more than 300-fold of the tiny 1-inch wafer 50 years ago.

Type	Diameter [mm]	Thickness [μm]	1st flat [mm]	Bowing [μm]
6 inch	150±0,5	≈700	55-60	25
8 inch	200±0,5	≈700	55-60	25
12 inch	300±0,5	≈700	55-60	25

Tab. 1.1: Typical data of wafers

With larger wafers, the throughput rate increases significantly in the manufacture of microchips, whereby the cost is reduced accordingly in the production. Thus, with identical structure sizese more than twice as many chips can be produced on a 300 mm wafer as on a 200 mm wafer. In addition, with increasing diameter the wafer's edge is less curved and thus the cut-off minimized (since chips are off rectangular shape).

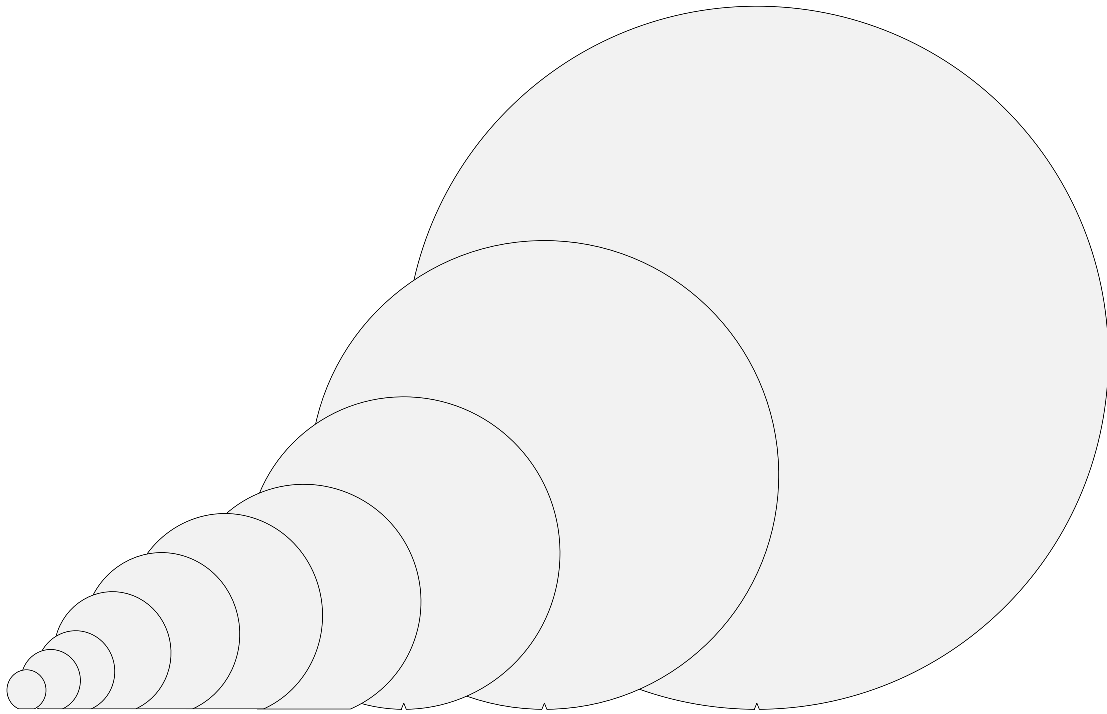

Fig. 1.4: Different wafer sizes: 25, 38, 51, 75, 100, 125, 150, 200, 300, 450 [mm] (drawn to scale)